Design of Low Noise Amplifier for 1.5 GHz

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Abstract

Low Noise Amplifier (LNA) is a front-end device of a radio frequency (RF) receiver used to increase the amplitude of an RF signal without much additional noise, thereby increasing the noise figure of the system. This paper presents design, simulation, and prototype of an LNA operating at 1.5 GHz for the bandwidth of 100 MHz. The circuit was simulated using Advanced Design System (ADS). The components used are Surface Mount Devices (SMDs); with transistor "Infineon BFP420" as a major component. Other components are resistors, capacitors, and inductors; inductors being superseded by microstrip lines. The circuit was fabricated on FR4 board. The measurements of several parameters of LNA were made using Vector Network Analyzer (VNA), Noise Figure Meter, and Spectrum Analyzer. The LNA has minimum gain of 15.4 dB and maximum noise figure of 1.33 dB. It is unconditionally stable from 50 MHz to 10 GHz. DC supply is 5V and the current consumption is 10 mA. This LNA offers Output-Third-Order-Intercept-Point (OIP3) of about 14 dBm.

Keywords : *Low noise amplifier, Advanced design system*

I. Introduction

LNA is an essential device in wireless communication systems such as satellite and mobile communication systems. It is used in receiver as a front-end device as shown in Fig. 1. Providing high gain to the RF signal and adding low noise decreases the overall noise figure of the receiver as suggested by Friis formula,

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \cdots G_{n-1}} \qquad (1)$$

where F_1, F_2, F_3, and F_n are the noise factors of the first, second, third, and the nth block of the cascaded system. And, G_1, G_2, G_3, and the G_n are the corresponding gains. Noise factor in dB scale is called the noise figure. Decreased overall noise figure is the reason why the use of LNA and its placement in the beginning is preferred in wireless systems.

The position of LNA in a heterodyne receiver is illustrated in the Fig. 1. The receiver mainly consists of antenna, band-pass filter (BPF), LNA, mixer, oscillator, and voltage gain amplifier (VGA).

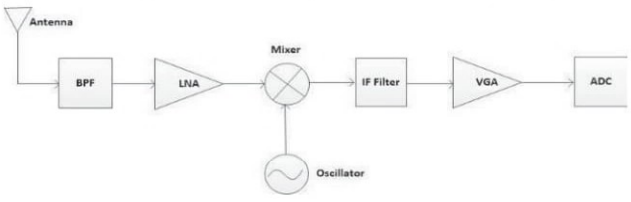

Fig. 1 Block diagram of heterodyne receiver. [1]

This paper includes the design, simulation, and prototype of an LNA operating at 1.5 GHz with bandwidth 100 MHz. The amplifier consists of transistor, resistors, capacitors, and inductors. All the components are SMDs: "Infineon BFP420" Bipolar Junction Transistor (BJT), 0603 capacitors and resistors. Appropriately calculated microstrip lines were used to mimic the inductors.

II. Literature Review

Different papers were reviewed to embark this project work. Most of the LNA designs were found to be based on CMOS technology with cascode structure. The paper [2] presents CMOS LNA design at 5.7 GHz with gain 11.45 dB and noise figure 3.4 dB. Another work at 5 GHz has gain 9.2 dB and noise figure 2.8 dB [3]. The design at 2.4 GHz has comparable gain of 11.2 dB and noise figure of 2.3 dB [4]. The paper [5] compares the performance of CMOS LNA and BJT LNA at 1 GHz. In this paper, the gain and noise figure of CMOS LNA was obtained as 21.64 dB and 1.78 dB respectively with the expense of huge power 23 mW; whereas the gain and noise figure of BJT LNA was achieved to be 14.3 dB and 1.87 dB respectively with the expense of only 4.6 mW. After analysing the performances of all the above LNA designs, I got motivated to design a simple BJT LNA with better performance at different frequency.

III. LNA Specifications

In practice, the specifications are made first before designing a device depending on its use. The important parameters for LNA are stability, gain, noise figure, input return loss, output return loss, and linearity.

A. Stability

LNA must be unconditionally stable for all passive source and load impedances. Stability can be described by μ-factor which is calculated using S-parameters as given below

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} \qquad (2)$$

where

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

For amplifier to be unconditionally stable, μ must be greater than 1. The frequency range for stability was chosen from 50 MHz to 10 GHz. [6]

B. Gain, Noise Figure, Input Return Loss, and Output Return Loss

Maximum available gain and minimum possible noise figure of BFP420 at 1.5 GHz are 20 dB and 1.1 dB respectively if the supplied collector current is 10 mA [7]. If input and output ports of LNA are simultaneously conjugate matched then maximum gain is possible. Input should be matched to Z_{OPT} to achieve minimum noise figure [6]. And the resistive components used for stability introduce some additional noise. So, maximum gain and minimum noise figure cannot be achieved simultaneously. The safer margin was kept and minimum gain was specified to be 15 dB and maximum noise figure to be 1.5 dB.

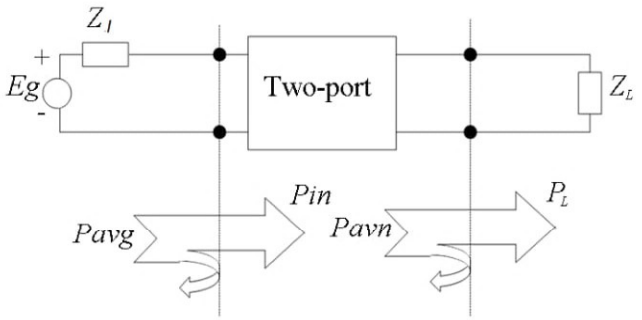

Fig. 2 Power notations in a two-port network.

In Fig. 2, P_{avg} is available power from source, P_{in} is input power to network, P_{avn} is available power from network, and P_L is power delivered to the load. When a signal goes to the input of a two-port network, some of its power gets reflected back due to the mismatch between source impedance and input impedance. Similar is the case in the output port. The reflection of wave at interface can be described in terms of return loss. The value of return loss becomes high if the impedance matching is good. Since input was targeted for noise matching and output was for maximum gain, the input and output return losses were specified to be optimal, that is; minimum of 7 dB and 10 dB respectively.

C. Linearity

For an amplifier to be linear, the plot of output power versus input power must be a straight line with a slope of unity. The linearity persists over a limited range, and then the amplifier response begins to saturate providing less gain. The nonlinearity property produces harmonics and intermodulation products. The harmonic components can be filtered out; where as some of the intermodulation products of closely spaced frequencies

may occur within the bandwidth of the amplifier. They ultimately cause distortion to the signal.

The plot of output power for the first-order and third-order products versus input power in dB is shown in Fig. 3. The output power of the first-order product is linearly proportional to the input power with the slope of unity. On the other hand, the response of the third-order products has a slope of 3. For high input power, both of these lines show compression. When the idealized responses are extended with the dotted lines, they intersect at a point which is known as third-intercept point, denoted as IP3. At this point, first-order and third-order power are equal. The intercept point is specified as either an input power level (IIP3) or an output power level (OIP3).

The third-order intercept point is a theoretical point that is never achieved in practice. The usefulness of this point lies while determining the linearity condition of an amplifier. The higher the output at the intercept, the better is the linearity and the lower is the intermodulation distortion (IMD). Third-order products are the most troublesome nonlinear effects for IMD and hence are studied most often. The IP3 value is an imaginary point that is never reached, as the amplifier will saturate before this condition can occur in practice. [6][8]

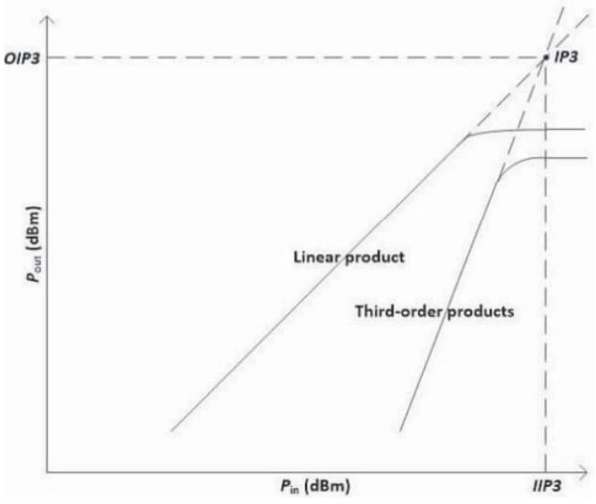

Fig. 3 Third-order intercept diagram for a linear device.

The rule-of-thumb for estimating the OIP3 is

$$OIP3\ [\text{dBm}] \approx 10\log_{10}\left(\frac{V_{\text{CEO}}I_{\text{CO}}}{1\ \text{mW}}\right) \qquad (3)$$

where V_{CEO} and I_{CO} are the quiescent collector-emitter voltage and collector current of a BJT, respectively, normally selected in the middle of the load line within IV-characteristic [9]. The specified values of V_{CEO} and I_{CO} in this project are 4V and 10 mA respectively. The use of this equation results 16 dBm as the approximated value for *OIP3*.

The Table I lists all the specifications mentioned in this section.

TABLE I
LNA SPECIFICATIONS

Parameter	Value
Gain (dB)	15 (min.)
Noise Figure (dB)	1.5 (max)
Input Return Loss (dB)	7 (min.)
Output Return Loss (dB)	10 (min.)
OIP3 (dBm)	16

IV. Simulations

Simulation was performed using ADS. Stability issue was sorted out first and other specifications were met after fine tuning of different components.

A. DC Bias Simulations

Current gain (β) of BJT420 model [7] in ADS was determined by using BJT-curve tracer utility in ADS. It was calculated to be approximately 73.

Collector-feedback bias was used in the amplifier design as shown in Fig. 4. The values of collector resistance (R_C) and base resistance (R_B) were calculated using the following equations; provided that the collector current was 10 mA and collector-emitter voltage was 4V.

$$I_{\text{B}} = \frac{I_{\text{C}}}{\beta},\ R_{\text{C}} = \frac{V_{\text{CC}} - V_{\text{CE}}}{I_{\text{C}}},\ R_{\text{B}} = \frac{V_{\text{CE}} - V_{\text{BE}}}{I_{\text{B}}} \qquad (4)$$

The calculated values were R_C = 100 Ω and R_B = 21.8 kΩ.

B. S-Parameters Simulations

S-parameter file of BFP420 provided by the manufacturer was used for S-parameters simulations [7]. The circuit diagram is shown in Fig. 5.

1) Substrate: Two-sided FR4 board was used as a printable circuit board with the parameters:

substrate thickness of 0.8 mm, substrate relative permittivity of 4.5, copper thickness of 17.5 µm, and loss tangent of 0.01.

2) ***DC Block:*** 0603 SMD capacitors were used as DC blocks. The graph as shown in Fig. 6 was used to determine the value of capacitance that is resonant at 1.5 GHz. It is clear that 22 pF must be the optimal value of capacitance.

3) ***RF Choke:*** RF choke or DC feed is used to prevent RF leakage to DC source but it offers negligible impedance for DC flow. In this project, it is implemented with one 22 pF capacitor and one quarter-wave transformer at 1.5 GHz. The length of the transformer was determined to be approximately 28 mm.

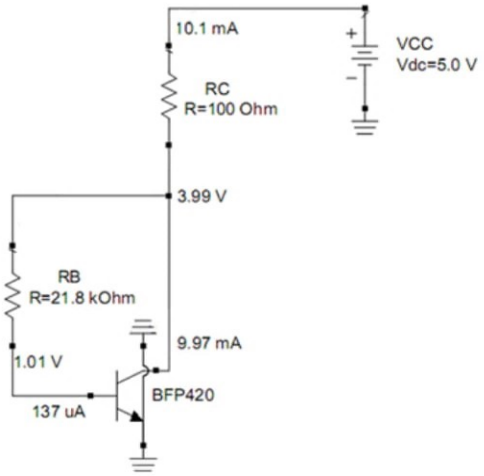

Fig. 4 DC biasing of BFP420.

C. Stability

A shunt resistor (R_{stab1}) and a series resistor (R_{stab2}) as shown in Fig. 5 under the stabilization network were used to make the amplifier unconditionally stable from 50 MHz to 10 GHz.

D. Input and Output Matching

It was fortunate that the input section was already noise matched without adding any matching network as shown in the Smith chart of Fig. 7. Output matching network in Fig. 5 with a capacitor and a shunted inductor was added to maximize the gain. The output section was conjugate matched depicted by the Smith chart as shown in Fig. 8.

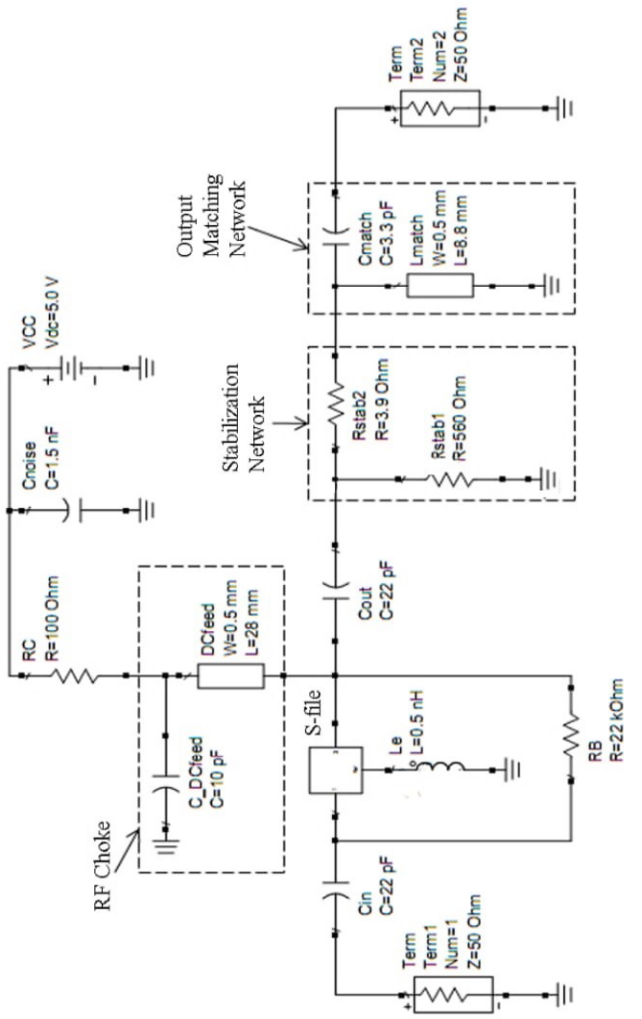

Fig. 5 Circuit diagram of LNA.

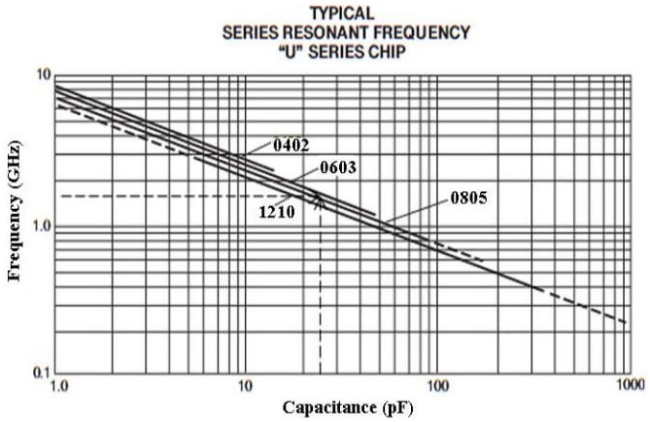

Fig. 6 Capacitor values at resonance. [10]

V. Prototype

After the completion of simulations, a layout was created as shown in Fig. 9. It has size of 27.5 mm × 27.5 mm ≈ 7.6 cm^2. It was designed such that its size was as small as possible without affecting its performance. The layout was printed on FR4 board and final product was constructed as shown in Fig. 10.

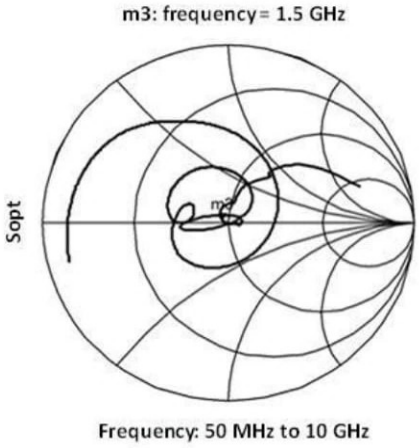

Fig. 7 Plot of Z_{opt} on Z_s line.

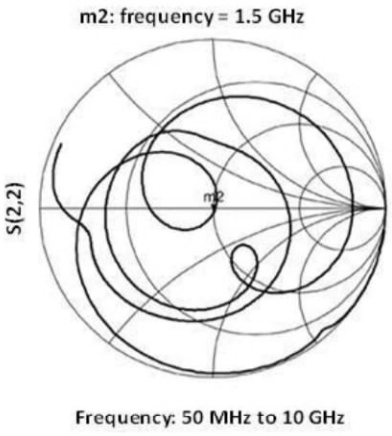

Fig. 8 Plot of S_{22} after matching network.

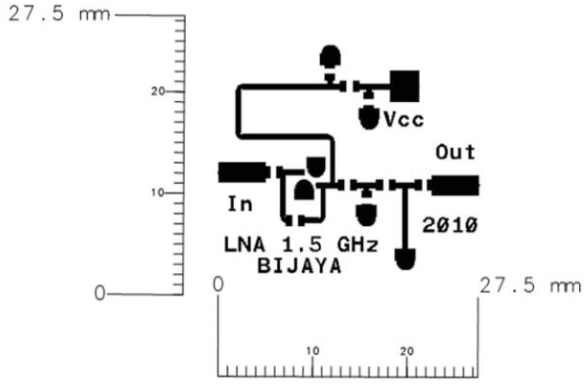

Fig. 9 Layout of 1.5 GHz LNA.

Fig. 10 Prototype of 1.5 GHz LNA.

VI. Results

This section presents the simulations results and the results from the measurements of the LNA prototype. To get the proper DC bias point of the prototype, the value of base resistor had to be increased to 33 kΩ from its simulated 22 kΩ. To get the parameters' values close to the simulated results, the output coupling capacitor Cout had to be decreased to 2.2 pF and capacitance of DC feed to 10 pF.

The VNA was used to measure the stability factor, gain, input return loss, and output return loss of the LNA. Similarly, the noise figure meter was used to determine the noise figure. And, the OIP3 measurement was carried out with the help of spectrum analyzer. The simulated and measured plots have been included in the same figure so as to ease the comparison analysis.

The plot of stability factor is shown in Fig. 11. This depicts clearly that the LNA is unconditionally stable within the range of 50 MHz to 10 GHz.

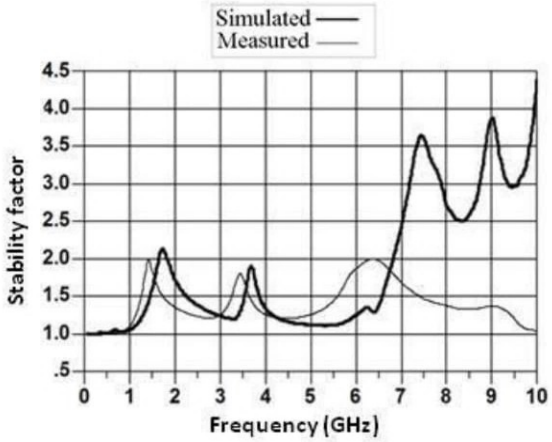

Fig. 11 Stability factor.

The results of gain, noise figure, input return loss, and output return loss are presented respectively in Fig. 12, 13, 14, and 15 respectively. The values of these parameters have been listed in Table II. In the table, 'S' represents 'simulated' and 'M' represents 'measured'.

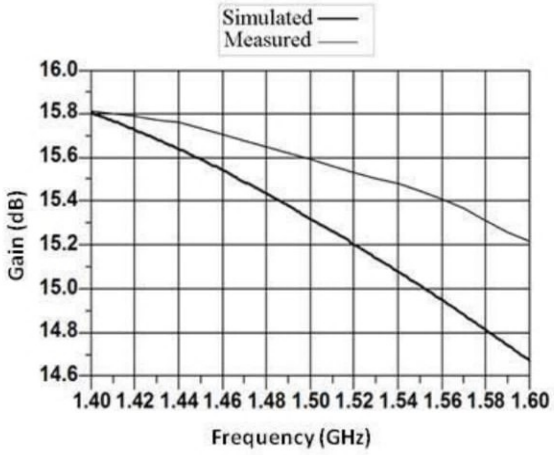

Fig. 12 Gain of LNA.

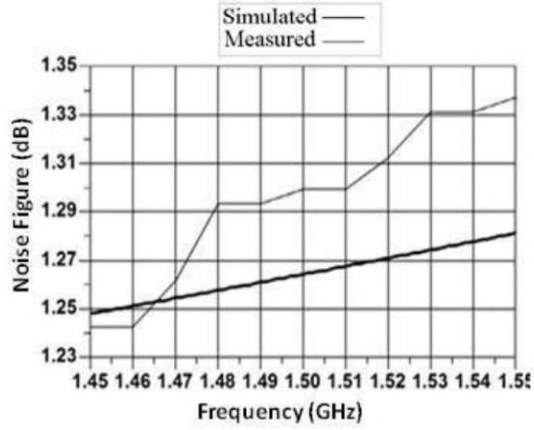

Fig. 13 Noise figure of LNA.

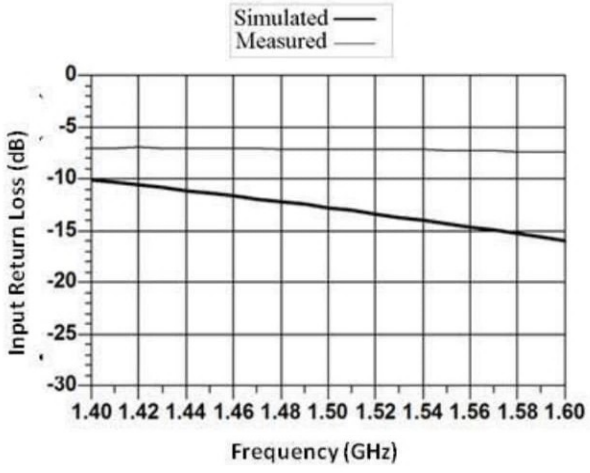

Fig. 14 Input return loss of LNA.

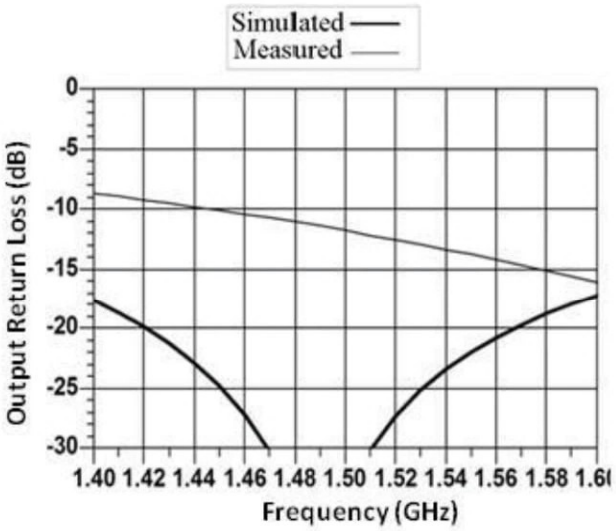

Fig. 15 Output return loss of LNA.

TABLE II
Results

Parameter	1450 MHz		1500 MHz		1550 MHz	
	S	M	S	M	S	M
Gain (dB)	15.6	15.7	15.3	15.3	15	15.6
Noise Figure (dB)	1.25	1.24	1.26	1.3	1.2	1.34
Input Return Loss (dB)	10	7	12.5	7.2	14	7.3
Output Return Loss (dB)	25	10	34.5	12	20	14

While comparing the results between simulations and measurements, we do not see much difference in gain and noise figure. On the other hand, the difference is prevalent for input return loss and output return loss. This might have resulted due to change in the value of coupling capacitor in the output section. However, both the simulated results and measured results have fulfilled the specified values.

Nonlinear model of transistor was used for the simulations of OIP3. The simulations results are shown in Fig. 16 for three frequencies: 1450 MHz, 1500 MHz, and 1550 MHz.

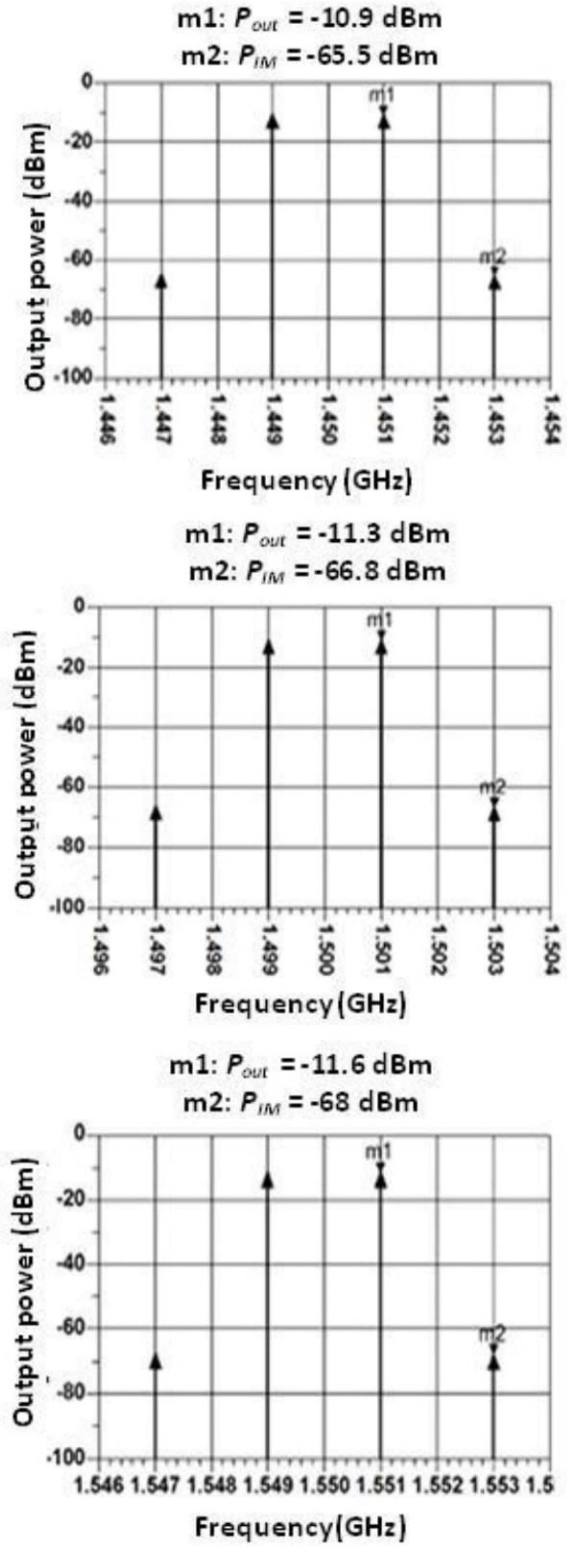

Fig. 16 Simulations results of OIP3.

Here, P_{out} is the fundamental output power and P_{IM} is the third-order intermodulation power. OIP3 can be calculated using

$$OIP3 = P_{out} + (P_{out} - P_{IM})/2 \quad (5)$$

Two signal generators and one spectrum analyzer were used to measure OIP3 at 1450 MHz, 1500 MHz, and 1550 MHz. The input power level was set at -20 dBm and fundamental power (P_{out}) and third-order intermodulation power (P_{IM}) were measured. The necessary data and the calculated OIP3 are tabulated in Table III.

TABLE III
OIP3 Calculations

Parameter	1450 MHz		1500 MHz		1550 MHz	
	S	M	S	M	S	M
P_{out} (dBm)	-10.9	-9	-11.3	-9.2	-11.6	-9.6
P_{IM} (dBm)	-65.5	-55	-66.8	-57	-68	-58.3
OIP3 (dBm)	16.4	14	16.45	14.7	16.6	14.75

The simulated OIP3 has minimum value of 16.4 dBm, whereas, only 14 dBm has been recorded as the minimum measured OIP3. So, the actual value differed from the specified one by 2 dBm.

VII. Conclusion

The specifications were prepared before designing the LNA at 1.5 GHz for the bandwidth of 100 MHz. The SMD components were used with BFP420 BJT transistor and 0603 resistors and capacitors. The inductors were implemented using the properly calculated transmission lines. The amplifier was simulated, and proper tuning of the components was made to meet the specifications. The LNA was fabricated on the FR4 board. By changing the values of few components, all the specified values of the parameters were obtained. The prototype is unconditionally stable from 50 MHz to 10 GHz. The minimum gain of 15.3 dB, the maximum noise figure of 1.34 dB, the minimum input return loss of 7 dB, and the minimum output return loss of 10 dB were obtained after measuring the LNA prototype. The minimum value of OIP3 was obtained to be 14 dBm. Except OIP3, all the parameters met the specifications. Such design can be used to develop LNAs at desired frequencies for mobile communication, satellite communication, and other forms of wireless communication where higher gain is required with the addition of very less noise. The gain can be increased further with multistage configuration.

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