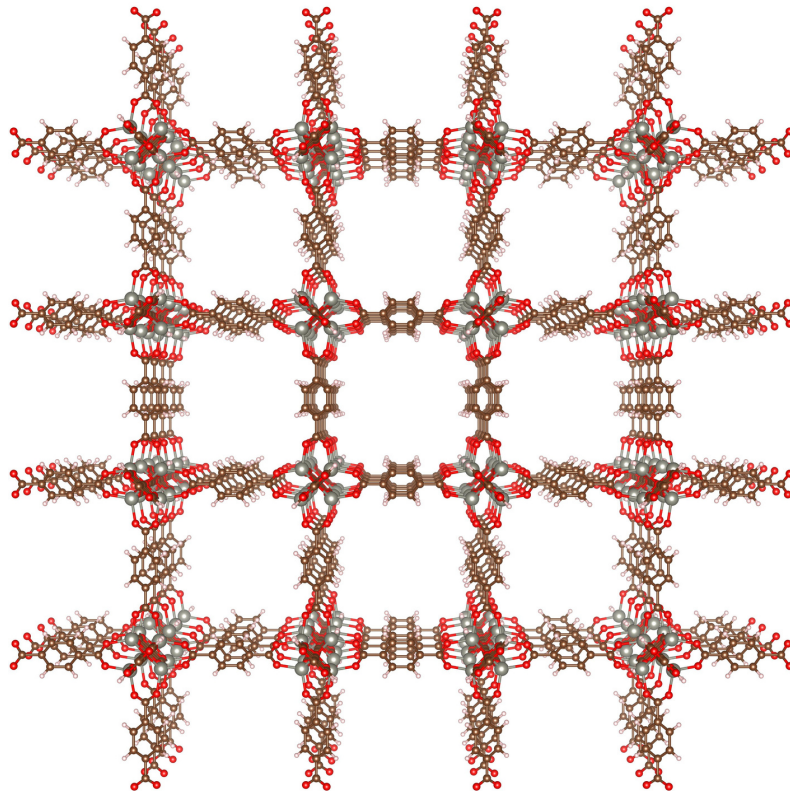


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*Cover: Ball-and-stick model of MOF-5. © Roshani Sharma. Printed with permission.*

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# Experimental design for tri-state logic

Research Article

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**Abstract:** Tri-State Logic device effectively connects many devices into the same data line for data transfer. The Tri-State TTL inverter has three output states such as LOW, HIGH, and open or high-impedance (High-Z) states. The High-Z state either electrically isolates the devices from the data transmission line or connects them one at a time to the data transmission line. The measurement of the floating output (opened or disconnected) state is a challenging task. This issue can be resolved by introducing a potential divider into the output of the original Tri-State TTL inverter circuit and making it possible for a lab experiment

**Keywords:** Data transmission • Tri-State Logic • High-Z • TTL • Inverter

## I. Introduction

In digital electronics, data transmission is a prime concern. The data transmission between multiple devices needs switches to be connected and disconnected frequently. If one performs it manually, the system will be slow and unreliable. In this sense, the network will be quite complicated and expensive. On the other hand, the digital data transmission system requires an automatic, fast, reliable, and comparably inexpensive simplified network. To achieve these requirements, a Tri-State Logic system came into existence [1–3], though its name is misleading because it does not use digital logic with three voltage levels [4].

The beauty of the Tri-State Logic gate is that it has an extra logic state called High-Z (high impedance) state in addition to the ordinary digital logic states LOW (0) and High (1). The High-Z state is equivalent to an electrically open (disconnected) state, which makes it possible to share the same line or bus for multiple devices with reliable great speed data transmission [5–7]. Thus, the Tri-State Logic gate became a trademark of National Semiconductor Corporation [4]. The modified TTL (transistor-transistor logic) inverter for Tri-State Logic is shown in Fig. 1 and its corresponding truth table is shown in Table 1 [3, 8]. This modified Tri-State Logic gate is easy to use in the laboratory because of its simplified circuit. However, it is equally difficult to distinguish or realize between the difference between LOW (0) state and a High-Z state because an ordinary voltmeter displays 0 V for both logics.

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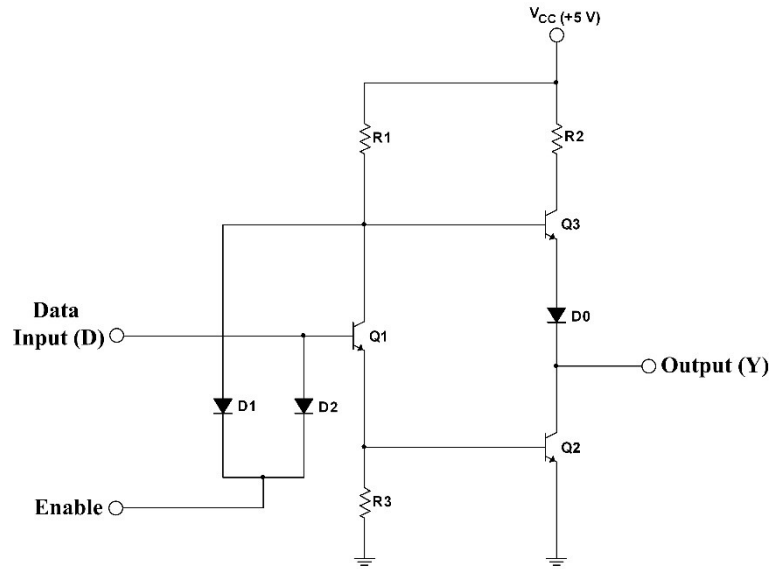


Figure 1. Tri-State TTL inverter.

Finally, we have added an extra resistor branch in the output side of the Tri-State Logic gate to remove the ambiguity between the LOW (0) and High-Z states, which enables the modified Tri-State Logic circuit as a lab experiment. The Tri-State TTL inverter circuit, one of many Tri-State devices, is used as a model for explanation purposes in this study.

Table 1. Truth table for a Tri-Sate TTL inverter

Enable	Data Input (D)	Output (Y)
0	0	Hi-Z
	1	Hi-Z
1	0	1
	1	0

## II. Experimental Design and Working

An experimental circuit of a Tri-State TTL inverter is given in Fig. 2. It is a modified version of the TTL inverter. The two diodes,  $D_1$  and  $D_2$ , are connected in such a way as to enable or disable the data for the output. All transistors are BC547B, all diodes are 1N4007, and all resistors with a 5% tolerance band are used to design the circuits.

### Condition 1: Enable HIGH (1)

When the Enable terminal is at the high-voltage (+5 V), both diodes  $D_1$  and  $D_2$  are effectively not participating in the circuit because both are in reverse biased conditions, and the remaining part of the circuit is

working as a TTL inverter with totem-pole output (R2-Q3-D0-Q2). This totem-pole output stage lowers the output impedance of the gate in the enable condition. In the totem-pole output configuration, both transistors Q2 and Q3 are driven into the cut-off and saturation regions in a complementary manner.

- When the Data input (D) is in the high-voltage (+5 V) state, both transistors Q1 and Q2 are driven into saturation. In this situation, the voltage at the junction of the collector of Q1 and the base of Q3 is nearly equal to 1 V with respect to the ground. The presence of D0 in the circuit ensures the cut-off condition of the transistor Q3 because the available 1 V potential is not sufficient to forward bias two diodes (D0 and the base-to-emitter diode of Q3). The saturated transistor Q2 provides the low-voltage ( $V_{CE(sat)} = \sim 0.2$  V) state for output.
- When the Data input (D) is in the low-voltage (0 V) state, both transistors Q1 and Q2 are driven into the cut-off region. In this situation, the transistor Q3 is driven into the saturation region as its common-emitter forward short-circuit current gain,  $\beta_F(\min) > 26$  (since,  $R1 = 2.2$  K $\Omega$ ), and diode D0 conducts. The saturated transistor Q3 pulls-up the output at a high-voltage ( $\sim 3.9$  V).

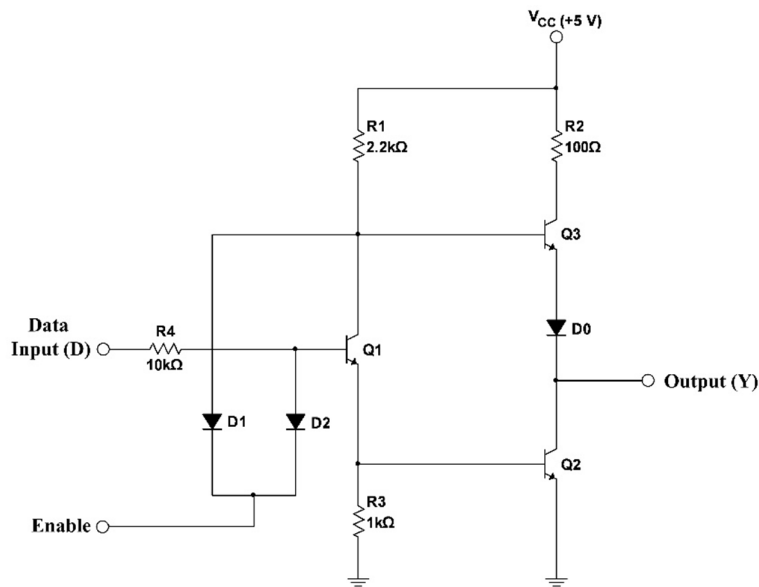


Figure 2. Experimental circuit for Tri-State TTL inverter

### Condition 2: Enable LOW (0)

When the Enable terminal is in the low-voltage (0 V) state, both diodes D1 and D2 pull down the base of transistors Q1 and Q3 to the LOW (0) level no matter what the input voltage-level is. For the silicon diodes the maximum forward bias voltage is 0.7 V. The maximum possible value of 0.7 V input to the base is not sufficient to drive two silicon diodes present in the loops (a)  $V_{BEQ1}$  and  $V_{BEQ2}$ ; (b)  $V_{BEQ3}$  and D0. In this situation, all three transistors Q1, Q2, and Q3 are driven into the cut-off region, and hence the output becomes floating i.e.,



disconnected from both  $V_{CC}$  and the ground. This condition is called a high-impedance (High-Z) output state because no current flows through the output terminal

### III. Results and Discussion

The observations of the experimental circuit given in Fig. 2 are presented in Table 2. All voltages were measured with a digital multimeter having a voltmeter of the least count = 0.01 V. The measured voltages are compared for their states with the TTL input-output profiles, which are shown in Fig. 3.

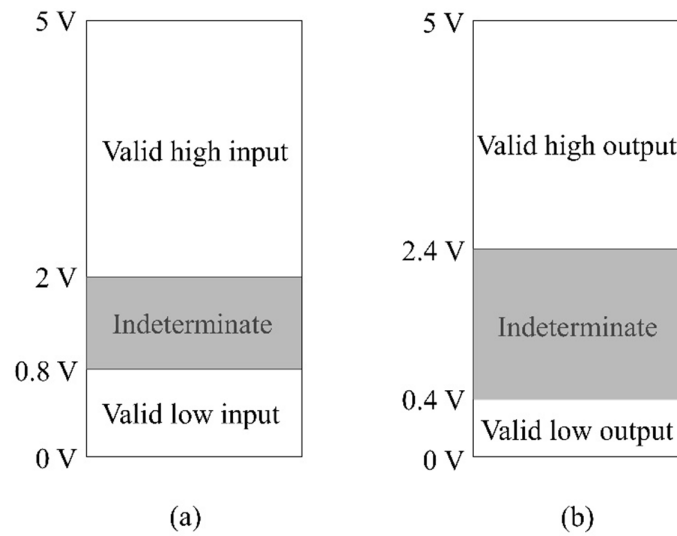


Figure 3. TTL (a) Input profile (b) Output profile.

When the Enable is HIGH (1) and the Data input (D) is LOW (0), the Output (Y) is in the HIGH (1) state. Also, for the Enable HIGH (1) and Data input (D) HIGH (1) the Output (Y) is observed in the LOW (0) state, which confirms the operation of the regular TTL inverter.

Table 2. Observation table for TTL Tri-State inverter circuit (without potential divider)

Enable	Data Input		Output	
	D	State	Y	State
0.00 V	0.00 V	0	0.13 V	0
	5.00 V	1	0.11 V	0
5.00 V	0.00 V	0	4.20 V	1
	5.00 V	1	0.01 V	0

Furthermore, in the Enable LOW (0) and the Data input (D) LOW (0) or HIGH (1) the Output (Y) should

be at a High-Z state according to Table 1. However, the observation with this input combination shows a LOW (0) state, which creates confusion between the High-Z state and the LOW (0) state outputs. This confusion is due to the fact that the ordinary voltmeter displays 0 for 0 V measurements as well as for the no current condition (High-Z). Thus, when designing a lab experiment, it is critical to distinguish between the High-Z and LOW (0) states by measurements.

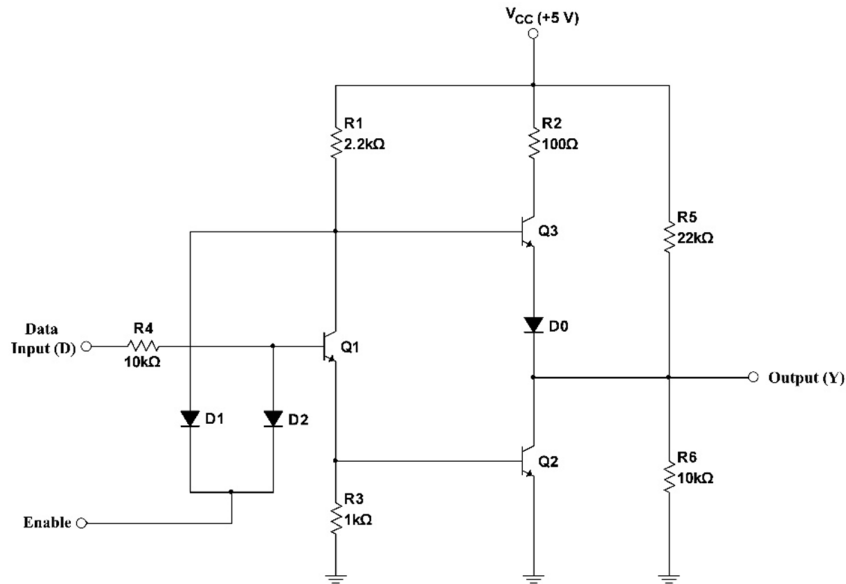


Figure 4. Experimental circuit for Tri-State TTL inverter (with potential divider)

### To distinguish the High-Z and the LOW (0) state:

As far as we know, the TTL Tri-State inverter's Output (Y) terminal cannot source or sink current in the High-Z state. Thus, a potential divider circuit with two resistors  $R_5$  ( $= 22 \text{ K}\Omega$ ) and  $R_6$  ( $= 10 \text{ K}\Omega$ ) is connected between the  $V_{CC}$  and the ground terminal of the circuit shown in Fig. 2, and the junction of  $R_5$  and  $R_6$  is connected to the output (Y), as shown in Fig. 4. Because current sourcing and sinking are not possible at the gate's output terminal under the High-Z state, the  $V_{CC}$  is simply split between the output potential divider circuit. Additionally, due to the large value ( $22 \text{ K}\Omega$  and  $10 \text{ K}\Omega$ ) resistors used in this supplementary potential divider circuit, the output impedance of the original circuit will not change in the enable condition.

Further, the observation table for the circuit shown in Fig. 4 is presented in Table 3. In Fig. 4, the Output (Y) is at 1.55 V, when the Enable is LOW (0) and the Data input (D) is either LOW (0) or HIGH (1). This value does not correspond to the LOW (0) or HIGH (1) state of the Output (Y) when compared to Fig. 3. This is for the High-Z state, which is deliberately designed to fall at an indeterminant level of the TTL input-output profile to distinguish it from the HIGH- and LOW-level outputs. This output result is only due to the potential division between resistors  $R_5$  and  $R_6$ . It means there are no sourcing and sinking effects of the transistors  $Q_2$  and  $Q_3$  to the output which ensures that both transistors  $Q_2$  and  $Q_3$  are in the cut-off conditions.

Table 3. Observation table for Tri-State TTL inverter circuit (with potential divider)

Enable	Data Input		Output	
	D	State	Y	State
0.00 V	0.00 V	0	1.55 V	High-Z
	5.00 V	1	1.55 V	High-Z
5.00 V	0.00 V	0	3.93 V	1
	5.00 V	1	0.02 V	0

Now, when the Enable is HIGH (1): (a) Data input (D) is LOW (0) and the Output (Y) is 3.93 V which is in a HIGH (1) state. Here, about 1 V is dropped across  $R_{32}$ ,  $V_{CEQ3(sat)}$ , and  $D_0$ . (b) With the same Enable HIGH (1) and the other input condition i.e. the Data input (D) is HIGH (1), and the Output (Y) goes to the LOW (0) state, which confirms the operation of the regular TTL inverter i.e. the output is the complement of its input.

Hence, the additional potential divider circuit in the output stage does not alter the normal operation of the TTL inverter circuit, also helps to measure the High-Z state and distinguish it from the usual HIGH- and LOW-level data. This small but important approach in the Tri-State TTL inverter makes it possible to study it as an experiment in the electronics laboratory.

## IV. Conclusions

The output of the Tri-State TTL inverter is either in a HIGH, LOW, or High-Z (or electrically disconnected) state corresponding to its Enable and Data input conditions. This High-Z output state of the Tri-State logic device allows sharing the same signal line or bus in the data transmission system without being short-circuited with other connected devices. However, the direct measurement of the voltage of the High-Z output state is misleading in the original Tri-State inverter circuit. The additional potential divider circuit in the output stage of the modified Tri-State inverter circuit is used to distinguish the LOW and High-Z states clearly. This modification allows for designing a Tri-State TTL inverter as a laboratory experiment, which helps to understand how devices can be connected and disconnected automatically in electronics.

Note: In the Large Scale Integration (LSI) system the open collector condition is automatically removed, and the additional resistor circuitry is not necessary.

## V. Acknowledgements

We would like to thank the electronics lab of the Central Department of Physics, Tribhuvan University, Kirtipur, Nepal.

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