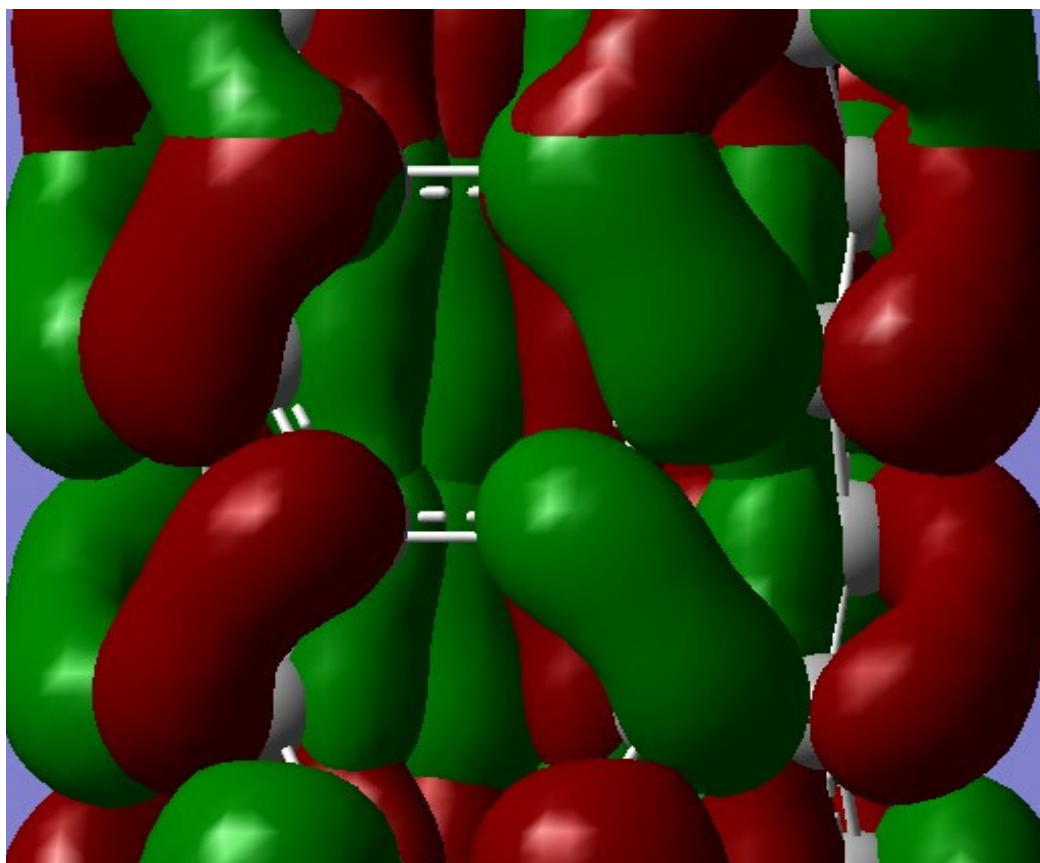


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An experiment study of etching of silicon in thermal environment

Research Article

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Abstract: Methods for the production of miniaturized mechanical components and devices in Silicon (Si) are available because micromachining methods are developed for the production of microcircuit. Moreover, complex shapes such as levers, gears and pinwheels have been produced through lithographic patterning coupled with etching methods. One of the electrochemical passivation techniques is discussed in the paper. A wafer with a particular impurity concentration is used and different impurities are diffused into wafer. This is done to form a diode junction at the boundary between the differently doped areas of silicon. The junction will delineate the structure to be produced. An electrical potential is then applied across the diode junction and the wafer is then immersed in a suitable wet etch by Potassium Hydroxide (KOH). This is done such a way that when etch reaches the junction an oxide layer is formed which protects the silicon from further etching. This is a kind of bulk micromachining technique. The main advantage of this technique is that much lower concentration of impurities is required, so that the resulting structure is more compatible with fabrication of microelectronic.

Keywords: Anisotropic etching • Chemical etching • Alkaline etchants • Etch rate

1. Introduction

Etching technologies in thin film processes play an important role in the semiconductor industry. Wet chemical etching techniques are used extensively in semiconductor processing because of their low cost, high throughput, and excellent selectivity. Important progress in the fabrication of microelectrical structure with integrated circuits has been achieved by many researchers using wet etching. For example, etchants based on hydrogen fluoride and water is widely used in treating silicon and silicon dioxide. Though detailed kinetic and electrochemical measurements have not been made, KOH solutions are extensively used for the etching of single crystal silicon [1–3]. Fabrication of U-shaped Metal Oxide Semiconductor (UMOS) transistors on Si (111) wafers for high power and high current densities has been achieved by applying KOH anisotropic wet etching to the silicon substrate[4]. Other applications of KOH wet etching include the fabrication of Vertical Metal Oxide Semiconductor Field Effect Transistors (VMOSFETs), radio frequency amplifiers, power supplies, and microcomputers [5]. Using its selective and anisotropic etching properties, KOH wet etching has also been applied to yield such

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devices as field emission devices, optical waveguide, pressure sensors, and ink nozzles[6–9]. KOH wet etching is one of the old anisotropic orientation dependent wet etching techniques. Etching of (100) oriented silicon using aqueous KOH creates V-shaped grooves with (111) planes at an angle of 54.74° from the (100) surface [4]. KOH solution can also be used to produce mesa structures[3]. There are several models proposed for the silicon etching mechanism in aqueous KOH[8–10]. The etching of single crystal silicon in aqueous KOH is of both technological and fundamental importance.

2. Methodology

The wafers used in this study were thermally bonded silicon on insulator (SOI) wafers with (100) orientation. The thickness of the top Si, buried SiO₂ layer and bottom Si were 2 and 250 nm respectively. The wafers were of p-type Si with a resistivity of 4-631022 Ω-cm for the top Si and 12-15 Ω cm for the bottom Si. Only the top Si layer was etched by the KOH solution. First, the SOI wafers were prepared with standard RCA cleaning. A 450 Å layer of Si₃N₄, which acts as a KOH etching mask, was deposited on each wafer using low pressure chemical vapor deposition (LPCVD). Oxide can be used as an etch mask for short periods in the KOH solution, but for a long period, nitride is a better etch mask as it etches more slowly. The SOI wafer was then cut into 10 mmx10 mm pieces. With the diced pieces held on a vacuum chuck, positive photoresist, OCG 825, was used to pattern the Si₃N₄ for the KOH etching mask. The nitride was etched with CF₄ plasma and then the exposed portion of the top Si on each SOI wafer was etched in KOH solutions of varying temperature and concentration. To assure the samples were free of particulate and other airborne contaminants, the experiments were conducted in a clean room environment.

3. Results and Discussion

The etch rate versus temperature and concentration observed as shown in Figs. (1a) and (1b). Fig. (1a) shows that etch rate increases with increasing reaction temperature. This plot would show three non-intersecting curves if there were no interaction between temperature and concentration in the etching reaction. However, since the curve for 20% KOH clearly intersects the 10% curve, this indicates that the etching rate is likely to depend upon some multiplicative function of temperature and concentration. Within the experimental range investigated, the etch rate exhibits a maximum at approximately 20% KOH and 90°C temperature. Below 70°C, little dependence of each rate with the KOH concentration was observed. Without considering the effect of etching, we conclude that the highest etch rate can be achieved with a high temperature reaction. Results demonstrate the effect of changing KOH concentration on the etch rate. It is observed that the effect of concentration is less statistically significant than that of reaction temperature. The wet chemical etching (KOH) of silicon is removal of silicon atoms in an alkaline solution. The final shape of the etched wafer depends highly on relative etching speed along crystallographic planes. The (111) plane is comparatively inert to alkaline etchants, while the relative etching

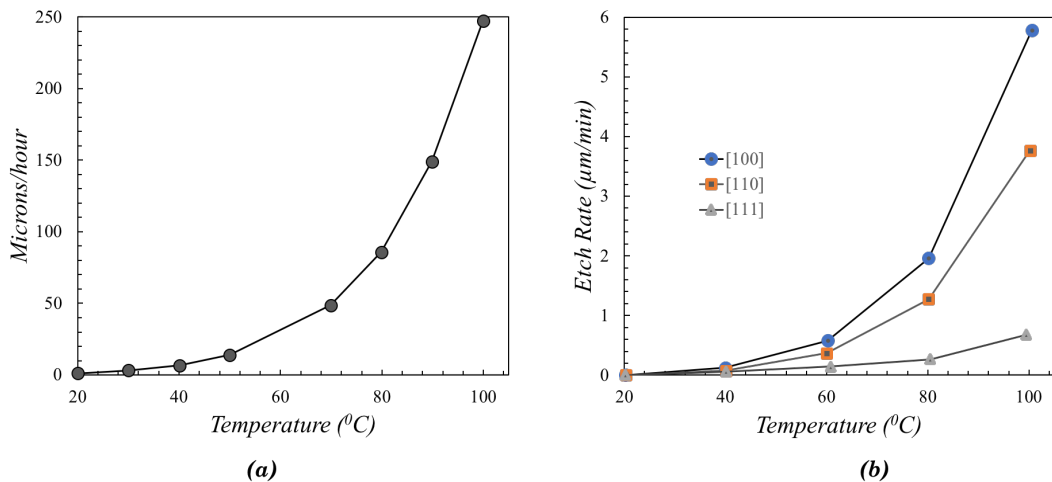


Figure 1. (a) The graphic relationship of etching rate with temperature for a 20% KOH by wt. (b) Variation of etch rate with temperature.

speed for other planes depends on etchant, temperature concentration, additives etc.

Table 1. Silicon etch rate ($\mu\text{m} \cdot \text{min}^{-1}$) in KOH for different concentrations and crystal orientations at an etching temperature of 70°C .

Crystal Orientation	Rates at diff KOH Conc.			Crystal Orientation	Rates at diff KOH Conc.		
	30%	40%	50%		30%	40%	50%
100	0.797	0.599	0.539	310	1.456	1.088	0.757
110	1.455	1.294	0.870	311	1.436	1.067	0.746
111	0.005	0.009	0.009	320	1.543	1.287	1.013
210	1.561	1.233	0.959	331	1.160	1.800	0.489
211	1.319	0.950	0.621	530	1.556	1.280	1.033
221	0.714	0.544	0.322	540	1.512	1.287	0.914

In our experiment, we have taken 33% KOH by weight as an etchant for silicon (111) and (100) crystallographic planes for anisotropic etching at ambient conditions, unless otherwise specified.

4. Conclusions

Anisotropic etching of Si with KOH is a well-known method of forming grooves in the Si surface. We report here the use of KOH solutions for etching silicon. Etching of (100) silicon on silicon on insulator (SOI) wafers was carried out over a wide range of reaction temperatures and KOH concentrations. We show that the factors important in the silicon etch rate are, reaction temperature, KOH concentration, and interaction between temperature and KOH concentration. In addition, in this work we report a qualitative study of the surface roughness of Si formed by KOH etching. The smoothness increases with temperature to a critical point and then

decreases at very high temperature and KOH concentration. Hydrogen bubbles formed during etching are very important in determining both etch rate and roughness. Results presented here are temperature dependent ER along the crystallographic orientations in silicon. Based on this work, temperature is crucial factor, which control ER. ER is slowest for the (111) face and fastest in the case of (110). Strong anisotropy in ER of KOH etching allow us a precious control of lateral dimension of the microstructure bound by the (111) planes.

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